A MODULAR INTERFACE DESIGN FOR A SMALL DIGITAL COMPUTER IN A HUMAN ENGINEERING LABORATORY

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THESIS

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by

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ABSTRACT

The design of a system interface for a PDP 8/E computer system and the research instruments of the Human Engineering Laboratory at the Naval Postgraduate School is discussed. Emphasis is on the digital logic where a modular approach is used. Each module is a common grouping of logic elements for performing a particular function. Seven function modules are described, and their integration into a complete system is discussed. It is intended that the equipment be built and the system tested in the near future.

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I. INTRODUCTION

In recent years digital computers have played an increasing role in research. At first, they were used primarily to analyze data resulting from experiments in all areas of research. More recently, the digital computer has moved into the laboratory to control and monitor the experiments, also.

In the early sixties the computer moved into the biological laboratory,[1] and in the late sixties into the psychological laboratory as evidenced by a series of articles on cybernetics in psychological journals by Karl U. Smith.[2]

The Human Engineering Laboratory at the Naval Postgraduate School currently has several research instruments, and has on order a PDP 8/E computer system. The objective of the research reported on in this thesis was to develop a system interface to link the research instruments to the computer. Five research instruments were considered, and the signals associated with the instruments were classified according to the type of parameter measured or controlled. Then, considering the electrical characteristics of the signals, an interface for each instrument was developed.

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[1]Schoenfeld, R. L. and Milkman, N., "Digital Computers in the Biological Laboratory," Science, v. 146, No. 3641, p. 190-198, 9 October 1964.

[2]Karl U. Smith has coauthored a number of articles on feedback control of auditory, visual, and physiological factors at the Behavior Cybernetics Laboratory, University of Wisconsin.

The emphasis of the work was on the digital interface logic needed to make some of the research equipment compatible with the computer. Logic elements, which consist of transistors, resistors, etc., and perform basic functions, were formed into seven function modules to perform more complex duties. The function modules were then combined to form each interface design.

This thesis begins with a classification of human factors in Section II. A listing of the research instruments and the parameters they measure, along with the signals available to the system, is included there, also. Section III describes the computer system and its features. After an introduction to the logic used, Section IV describes the function modules. In Section V, the integration of the function modules into an interface design for the human factors monitoring and control system is discussed. Finally, concluding remarks are given in Section VI.

II. MEASUREMENT AND CONTROL

A. GENERAL

The human subject may be considered a system with inputs and outputs (see Figure 1). The input would be the environment of the subject and the output would be the subject's evidence of behavior. The relationships between the inputs and the outputs give information about the basic life functions and higher order functions of man. These functions are very complex with a great dependence on time and feedback. If the functions can be established, man's actions can be predicted and used to best advantage in man-machine systems.

A human factors laboratory usually performs experiments with humans in man-machine situations to find relationships between the input and output factors. It then designs and tests equipment aimed at using these relationships best in man-machine systems.

The major problem in a human factors experiment is the measurement and control of the factors involved. In many cases the parameters have related signals with properties (such as small magnitude) that make them difficult to measure even with complex equipment. Other difficulties lie in the fact that some signals are obscured by signals from parameters other than the one in question. Another difficulty is that some parameters cannot be directly measured and must be measured through signals indirectly related to the parameter. In the control of the input factors one must consider the tradeoffs of complex equipment and the discrimination abilities of the senses.

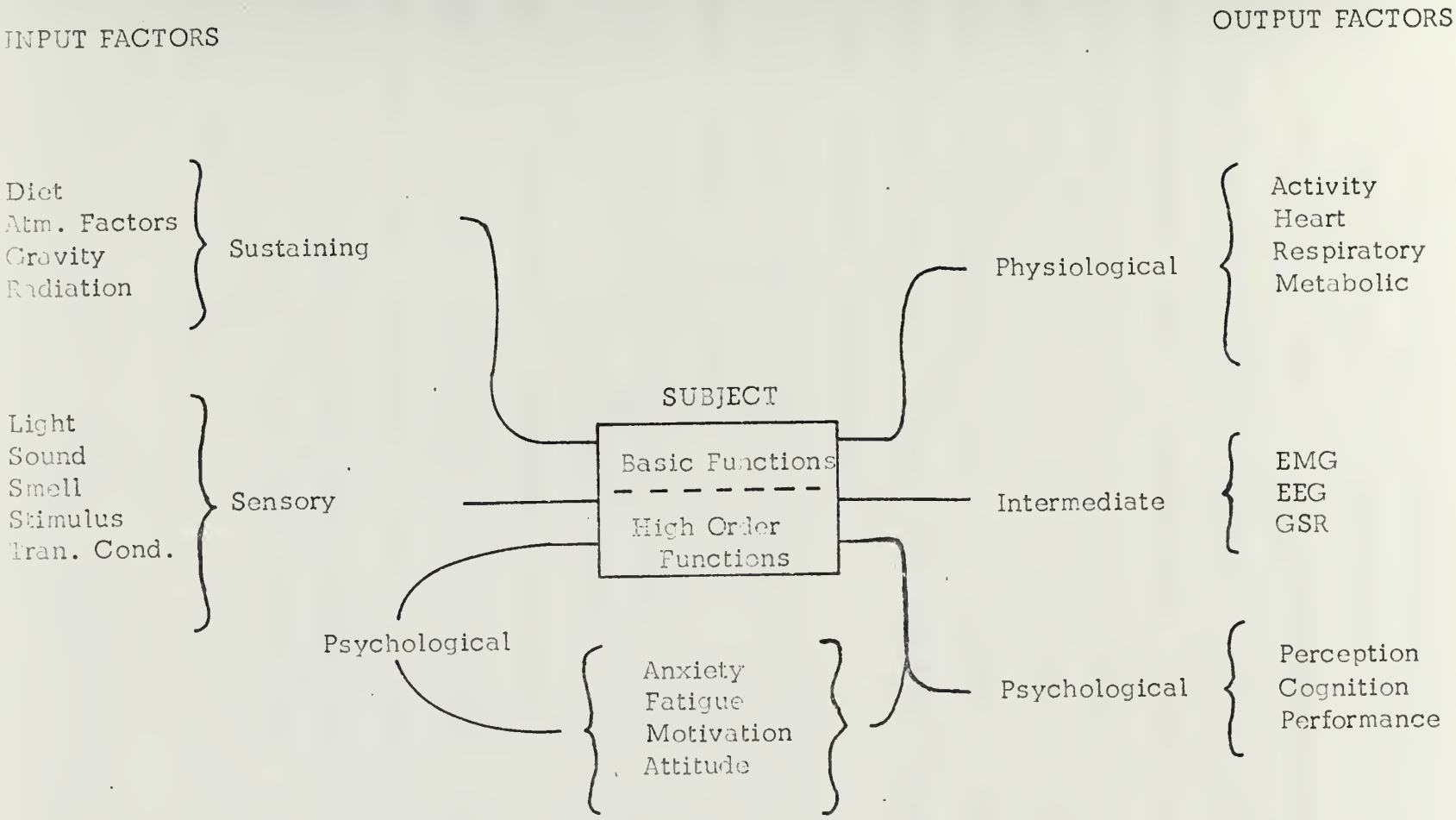

Figure 1. Human Input and Output Factors

B. CLASSIFICATION OF HUMAN FACTORS

The input (environmental) factors may be grouped into three categories--sustaining, sensory, and psychological. The sustaining factors are the important determinants of basic physiological behavior and generally nonsensory in their steady state conditions. These include diet, atmospheric factors, gravity, infectious agents, and radiation. The sensory factors which influence the higher order functions are light, sound, transient atmospheric conditions, and smell. The psychological factors--anxiety, fatigue and stress, reflex, inherent and learned behavior patterns, motivation, attitude, and others--are feedback from the subject influenced by past experience.

The output factors (evidence of behavior) may also be divided into three categories--physiological, intermediate, and psychological. Evidences of activity, respiratory and metabolic indices, heart activity, blood pressure, etc., are included in the physiological category. The psychological measures are the indices of perception, cognition, and performance. These include tracking, problem-solving, operant behavior, etc. The third group, intermediate, consists of the behavior measures that could be considered to be in both of the other groups. Such measures as skin responses (GSR), electroencephalographs (EEG), and electromyographs (EMG) are in this area.[3]

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[3] Technical Documentary Report No. AMRL-TDR-62-98 (1), Techniques of Physiological Monitoring: Volume I, Fundamentals, by Becker, W. L. and others, p. 1-5, September 1962.

C. SYSTEM FACTORS

The remainder of this chapter will enumerate the factors measured or controlled by the proposed system. The system will rely greatly on present equipment available at the laboratory to measure the factors.

Five instruments are to be integrated into a system with the computer. These are a polygraph, a Lifecycle, a treadmill, a pupilometer, and a human factors panel.

The polygraph is a four channel instrument with the appropriate transducers, couplers, and amplifiers to monitor an AC/DC signal, an EMG - direct or integrated, an EKG - direct and rate, skin temperature, and GSR. Of the six possible signals (two due to the EKG), only four may be monitored simultaneously. The output of the polygraph is analog with a range of 5V.

The Lifecycle has three significant signals to be monitored. These analog signals - crank RPM, pulse rate, and calories/hr - have an available range from 0 to .01mV, so they must be amplified to be compatible with the computer.

The treadmill provides one analog signal, the speed of the tread. This signal must also be amplified for compatibility.

The pupilometer provides an 8 bit word indicating the diameter of the pupil. It also provides two timing pulses - one positive going, one negative going - each 1.8 μs. The sample rate of measurement and timing strobe is 60Hz. The voltage levels are compatible with the interface logic.

The human factors panel provides a variety of stimulus and response units. The seven units consist of:

1. a telephone dial and switch
2. a dual 12 stimulus readout and switch
3. a 3X4 lighted key array
4. a 3X4 light array
5. a nonsense syllable panel
6. a score panel (digital counter and lamp)
7. a coin dispenser

These all either send or receive a two-state digital signal of 12V.

A breakdown into categories of the variety of parameters associated with these instruments is given in Table I. From the table, it can be seen that this system, if implemented, could be a major step toward a general automated human factors monitoring and control system.

Table I

Measures Available from Present Equipment

Type	Parameter	Instrument
Input		
Sensory	Stimulus	
	1. 3X4 light array	Human Factors Panel
	2. 3X4 lighted key array	
	3. symbol stimulus	
	4. nonsense syllable panel	
	5. score panel	
Psychological Motivation		
	coin dispenser	Human Factors Panel

Table I (cont)

Type	Parameter	Instrument
Output		
Physiological	EKG	Polygraph
	Temperature	Polygraph
	Pulse rate	Lifecycle
	Pupil diameter	Pupilometer
Intermediate	EMG	Polygraph
	EEG	
	GSR	
Psychological Performance		
	A. 1. 3X4 key array	Human Factors Panel
	2. switches	
	3. telephone dial	
	B. 1. crank RPM	Lifecycle
	2. calories/hr	
	C. 1. speed of tread	Treadmill

III. COMPUTER SYSTEM

A. SYSTEM

The following is a summary of the computer system to be used:

PDP 8/E central processor
8K memory
2 tape drives (2.7×10^6 bits/tape)
high speed reader/punch
real time clock
10 bit A/D converter
8 channel analog multiplexer
oscilloscope

B. COMPUTER

The computer will be the heart of the proposed system. Its purpose is to control the peripheral devices, then store and manipulate the data acquired.

The basic processor uses 12 bit, two's complement arithmetic. It is a single-address, fixed word length, parallel-transfer computer, having a single cycle time of 1.2-1.4 μs. Other features are indirect addressing and instruction skip capabilities.

C. INPUT/OUTPUT METHODS

There are three methods to transfer information to and from the central processor. The data break method transfers large blocks of data by direct transfers to and from the processor's memory. Since the proposed

system will usually require one and, at most, a few words of data at one time, the data break method (which needs considerable interfacing) would be uneconomical to use. The programmed data transfer method is a program initiated transfer of as many words as required. This method is slower than the data break method since it transfers data using the major processing registers under direction of a program. Characteristic of this method is the use of IOT instructions for sampling and clearing flags, skipping, clearing the accumulator, and reading, loading, and clearing buffers. The third method, program interrupt method, is a peripheral device initiated method. It allows the device to tell the processor that it is ready to transfer data. The processor checks which device requested the interrupt; then goes into a service routine for that device. The service routine is similar to the routines for transferring data in the programmed data method.

D. OMNIBUS

The Omnibus is probably the most important feature of the PDP 8/E for this application. It provides all the timing and transferring signals on an organized bus allowing plug-in elements availability to all signals. This saves space by allowing a high density of electronics, and it eliminates crosstalk between signals due to random wiring.

The signals of the Omnibus used in the programmed data and program interrupt methods are tabulated in Table II. These are not all of the signal lines available on the Omnibus but are the only lines pertinent to the programmed data and interrupt program methods of interfacing.

Each transfer must be made in one cycle (1.2 μs) or a timing generator for the BUS STROBE must be provided by the peripheral device. Figure 2 illustrates timing of the time pulses and time states.

E. EXTERNAL BUS

The External Bus is created by a Positive Bus Interface and Data Break Interface (optional equipment provided for the computer) which buffers and maps the Omnibus signals into a new set of signals compatible with peripheral devices designed for other computers of the PDP 8 family of computers. This bus may also be used to interface special peripheral equipment to the computer. This feature is not used in this system design since it requires hardware external to the computer.

F. A/D CONVERTER

With the computer will be an analog-to-digital converter with a multiplexer for 8 channels. The A/D converter is a 10 bit successive approximation type converter. The input to the converter is 0 to +10V with an input impedance of greater than 70K Ω in parallel with 300pF. The computer is capable of a 50KHz frequency rate. The multiplexer provides random or sequential selection of the analog channels. The input voltage is either 0 to +1.0V or 0 to -1.0V. Its impedance is 70KΩ in parallel with 300pF. It outputs to the A/D converter a 0 to 10V signal.[4]

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[4] Digital Equipment Corporation, PDP 8/E Small Computer Handbook, 1971.

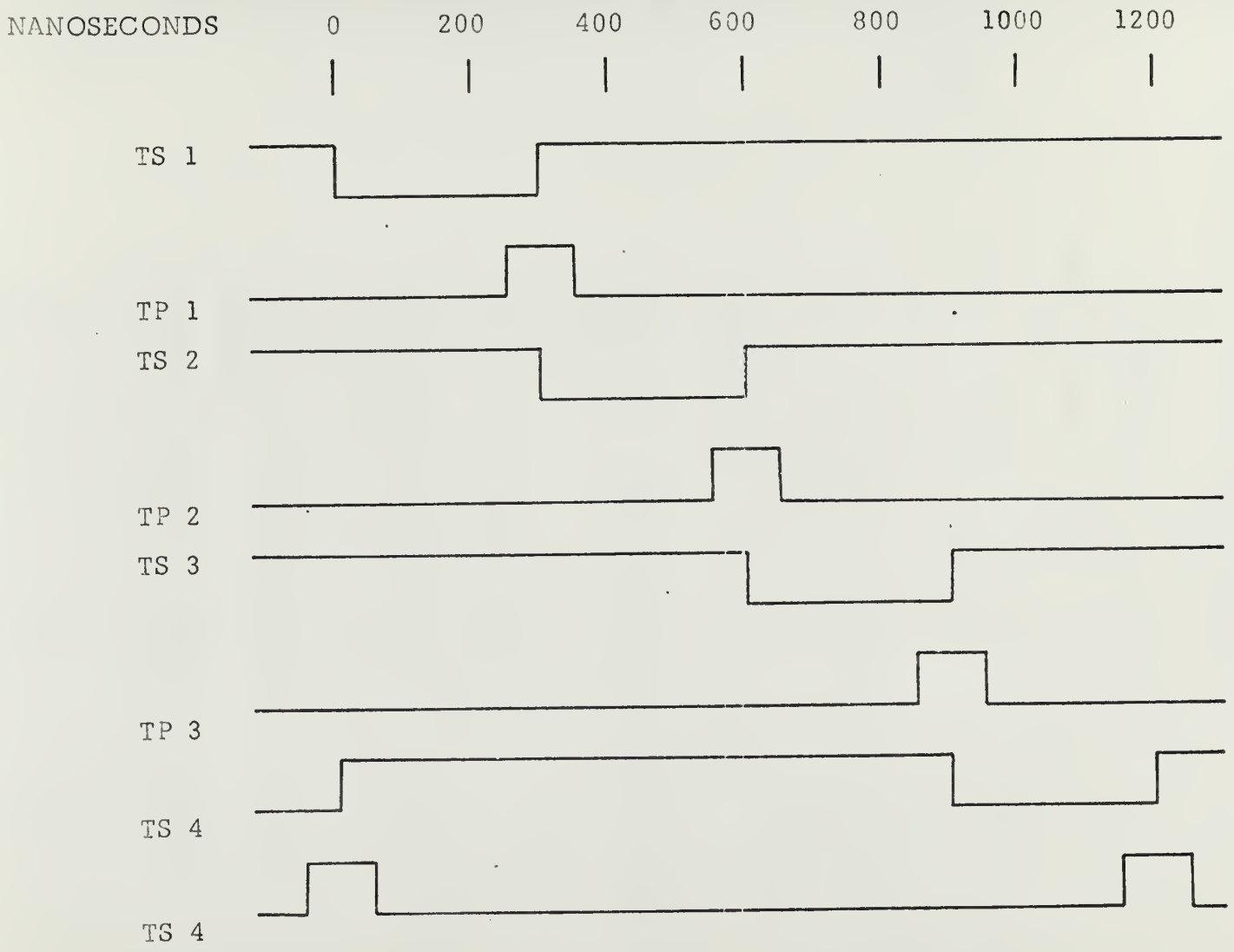


Figure 2. Timing Diagram for a Computer Cycle

Using the Omnibus and A/D converter and multiplexer, it is possible for all of the needed parameters of the Human Factors Laboratory to be interfaced to the computer. This requires the design of gating and timing circuits for the digital portions and either direct application of the analog signals or modifying them to meet the input requirements.

Table II

Omnibus Signals Lines

Signal Lines	Definition
DATA 0-11	DATA lines 0-11 are a bidirectional multipurpose bus. These lines are generally the input/output paths between the peripheral device and the accumulator register. At TS3 of the IOT instruction, they carry information to or from the AC according to CO-2. Low if asserted.
MD 0-11	Memory Data lines 0-11 carry information to and from memory. They carry the Device codes and IOP bits during an IOT induction. Low if asserted.
TP 1, 3	100nsec positive-going pulses for timing indicates a change of time state.
TS 1, 3	These lines indicate the appropriate time state. Time states are 200nsec or more in duration and change 50nsec after the leading edge of the associated time pulse. Low if asserted.
INITIALIZE	A positive-going pulse at least 600nsec long used to clear AC, LINK and all flags in the peripherals.
RUN	This line indicates the Central Processor is executing instructions. Negated at TP3 if the machine is stopped. Low if asserted.
I/O PAUSE	Asserted at TP2 of IOT cycle. Signifies an IOT is being processed. Used to gate signals in peripherals. Negated at LAST I/O XFER.

Table II (cont)

Signal Lines	Definition
INTERNAL I/O	Indicates whether the peripheral device is internal or external. Tells the Positive I/O interface to ignore IOP. Low if asserted.
CO, C1, C2	Controls the type of I/O transfer according to: CO C1 C2 Function H H H DATA V AC → AC L H H AC → DATA, 0 → AC H L H DATA V AC → AC L L H DATA → AC * H L DATA + PC → PC * L L DATA → PC *Don't Care
BUS STROBE	A negative-going pulse signifying an I/O transfer is taking place. Repeatedly generated by TP3 when NOT LAST XFER is asserted. BUS STROBE used for timing signals. When NOT LAST XFER is negated, BUS STROBE generates an INT STROBE.
NOT LAST XFER	Indicates that the next BUS STROBE does not terminate the I/O transaction. Low if asserted.
SKIP	This signal is sampled at TP3 of an IOT and causes Central Processor to skip the next instruction.
INT RQST	INT RQST is asserted by peripherals requiring service. Sampled at Interrupt Strobe time causes Central Processor to enter a service routine for the peripheral devices. Low if asserted.

IV. FUNCTION MODULES

This chapter will deal with the development of function modules. The function modules are constructed from basic logic elements. In interface designs several groupings of logic elements repeatedly appear. Thus the formations of the common groupings into function modules can ease the difficulties of detail in designing interfaces.

A. SIGNALS

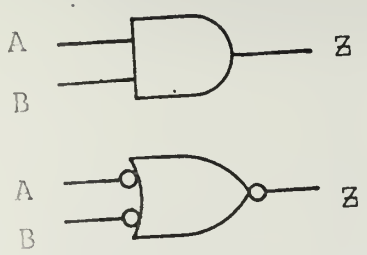
The interface modifies and manipulates signals between the external device and the computer. The signals are analog, voltage levels, or a series of pulses. The analog signals must be changed into either voltage levels or series of pulses compatible with the computer depending on their usage. The voltage levels and pulse series from the external device might have to be modified to be compatible with the logic voltage or to perform their intended function.

B. LOGIC ELEMENTS

To understand the construction of the function modules, Figures 3 through 5 give the symbol definition and truth tables for the basic logic elements. In this work a true state is signified by a 1, and a false state by 0.[5]

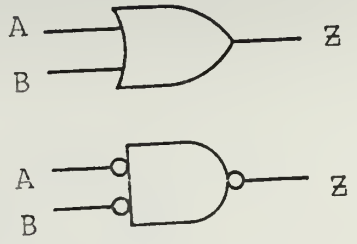
For ease in following the logic, two logic symbols appear for most of the gating elements. The significant characteristic is the placement

[5]Digital Equipment Corporation, Logic Handbook, p. 12-18, 1971.



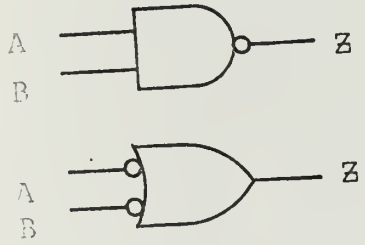
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate
All inputs must be 1 for the output to be 1.



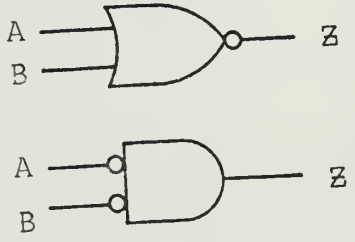
A	B	Z
0	0	0
0	1	1
1	0	1
0	1	1

OR Gate
All inputs must be zero for the output to be 0.



A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

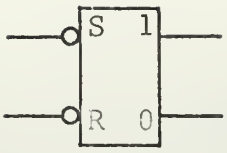
NAND Gate
All inputs must be 1 for the output to be 0.



A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

NOR Gate
All inputs must be 0 for the output to be 1.

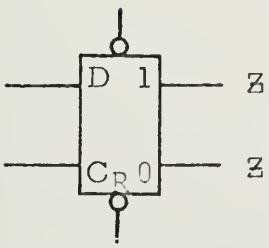
Figure 3. Basic Gating Elements



SR Flip-Flop

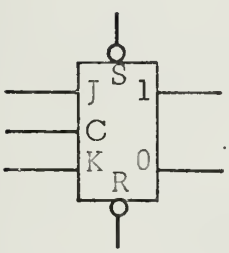
input conditions		output			
S	R	1	0	1	0
0	0	0	1	1	1*
0	0	1	0	1	1*
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	0	1	0

*The input that stays 0 longest assumes control.



Data Flip-Flop

The S & R inputs are the same as the SR FF. At the leading edge of the clocking signal at C, the signal on D determines the state of the FF. That is, if D is 1, Z is 1; and if D is 0, Z is 0.

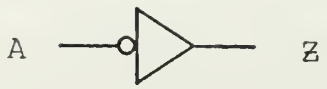


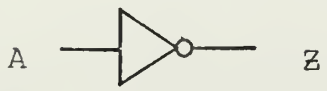
JK Flip-Flop

input conditions		output			
J	K	1	0	1	0
0	0	0	1	0	1
0	1	0	1	0	1
1	0	0	1	1	0
1	1	0	1	1	0
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	0	1	0
1	1	1	0	0	1

The S & R inputs are the same as in the SR FF.
The JK Flip-Flop triggers on the trailing edge of a positive-going pulse.

Figure 4. Basic Memory Elements



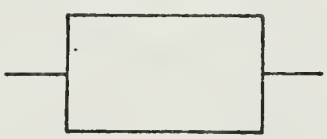


INVERTER

A	Z
0	1
1	0

The inverter changes the state of the signal.

This symbol indicates a conversion of voltage levels.



This symbol is used to indicate a general function.

Figure 5. Miscellaneous Elements

of a circle at the input and output lines of the basic symbol. This circle inverts the state of the line. (i.e., if an input line is 1 and enters a circle, it appears as a 0 to the basic symbols; and if the output of the basic symbol is 0 and leaves through a circle, the output of the complete symbol is 1)

C. MODULES

Seven common groupings of logic elements are used in the proposed system design. Each of these function modules is described in detail in the remainder of this chapter.

1. Device Selector

The device selector decodes the device code of an IOT instruction and enables the gating for the selected peripheral. It also tells the External Bus whether the selected device is internal or not (the External Bus then ignores the signal). Lastly, the device selector decodes the last three bits of an IOT instruction into eight signals used for gating, clearing of flags, and skipping.

MD 3-8 are gated with I/O PAUSE to enable the peripheral device. For a particular code the MD bits that are 1 must be inverted to be properly gated into the NOR gate. The signal then enables the gating for MD 9-11 and allows a NAND gate to assert the INT I/O line. MD bits 9-11 are decoded into eight IOT signals. (Figure 6)

2. Word Program-Timed Transfer

This module gates a set of signals into a SR memory register to be held until they are no longer needed. Gating and clearing is usually

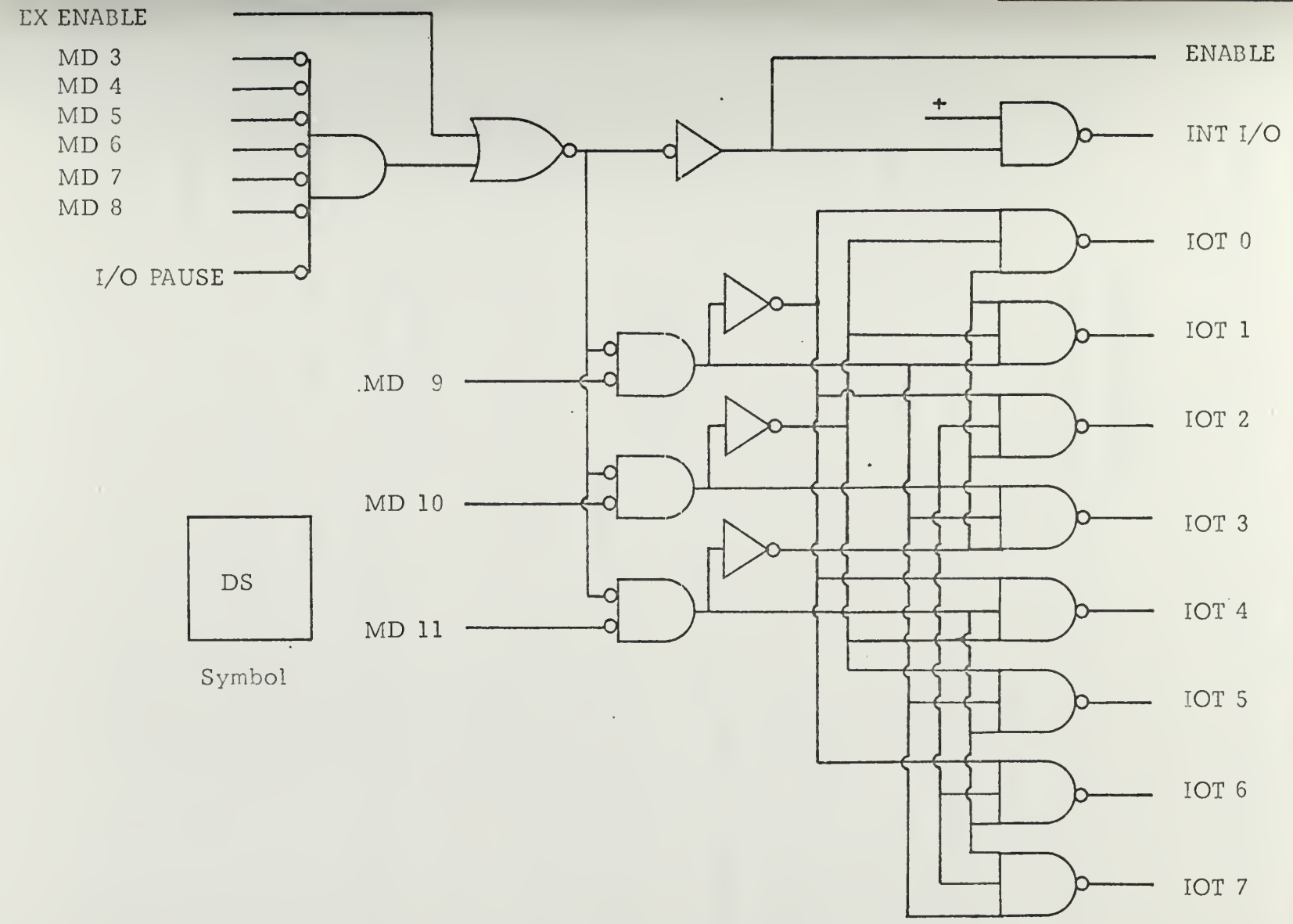


Figure 6. Device Selector

done under program control through the IOT instructions. When the READ IN line is 1, bits 0-n are gated into the SR flip-flops. A 0 signal on CLEAR resets the SR register to 0's. Both 1 and 0 signals are available on the output of the module. (Figure 7)

3. Word Jam Transfer

The word jam transfer module allows a word to replace a previous word in the memory register without being cleared first. This module is used in transferring information from the computer to the peripheral device. When TRANSFER ENABLE is pulled to 0, data is available to be clocked into the data flip-flops by TP3. The register may also be cleared by asserting CLEAR with a signal. The word in the register and its complement are available as outputs of the module. (Figure 8)

4. Read In Gating

Using TP3 and a signal from a device selector, this module gates a word in the peripheral device onto the Data Bus and directs it to the accumulator by asserting C0 and C1. (Figure 9)

5. Flag and Interrupt

The Flag and Interrupt module has two SR flip-flops whose signals are then gated to the INTRQST and SKIP lines. When the enable flip-flop is set, the flag flip-flop will cause INT RQST to be asserted. When the flag flip-flop is not set and an IOT is given, the next instruction in the program will be skipped. An output FL is given to aid in gating switches. (Figure 10)

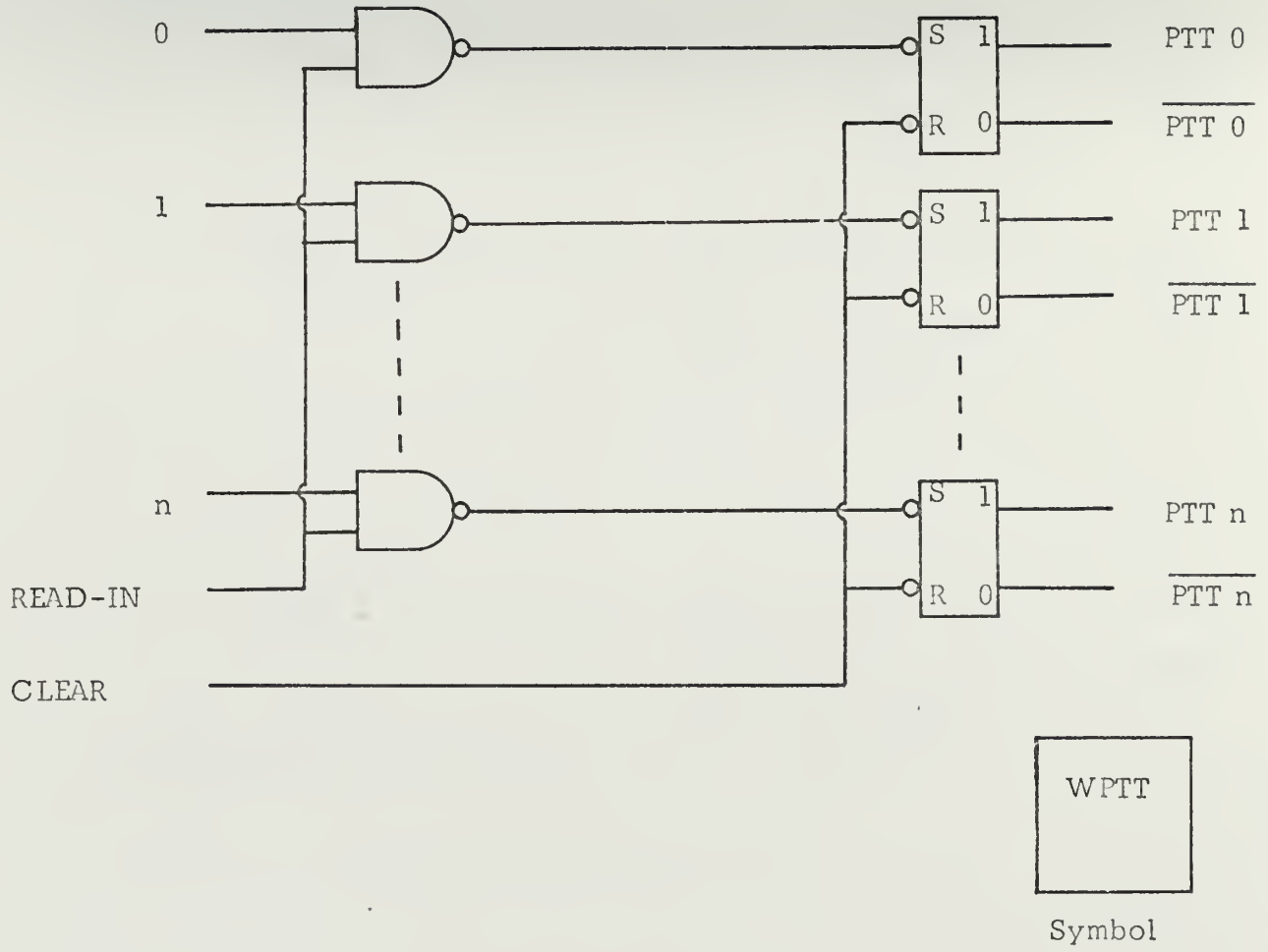


Figure 7. Word Program-Timed Transfer

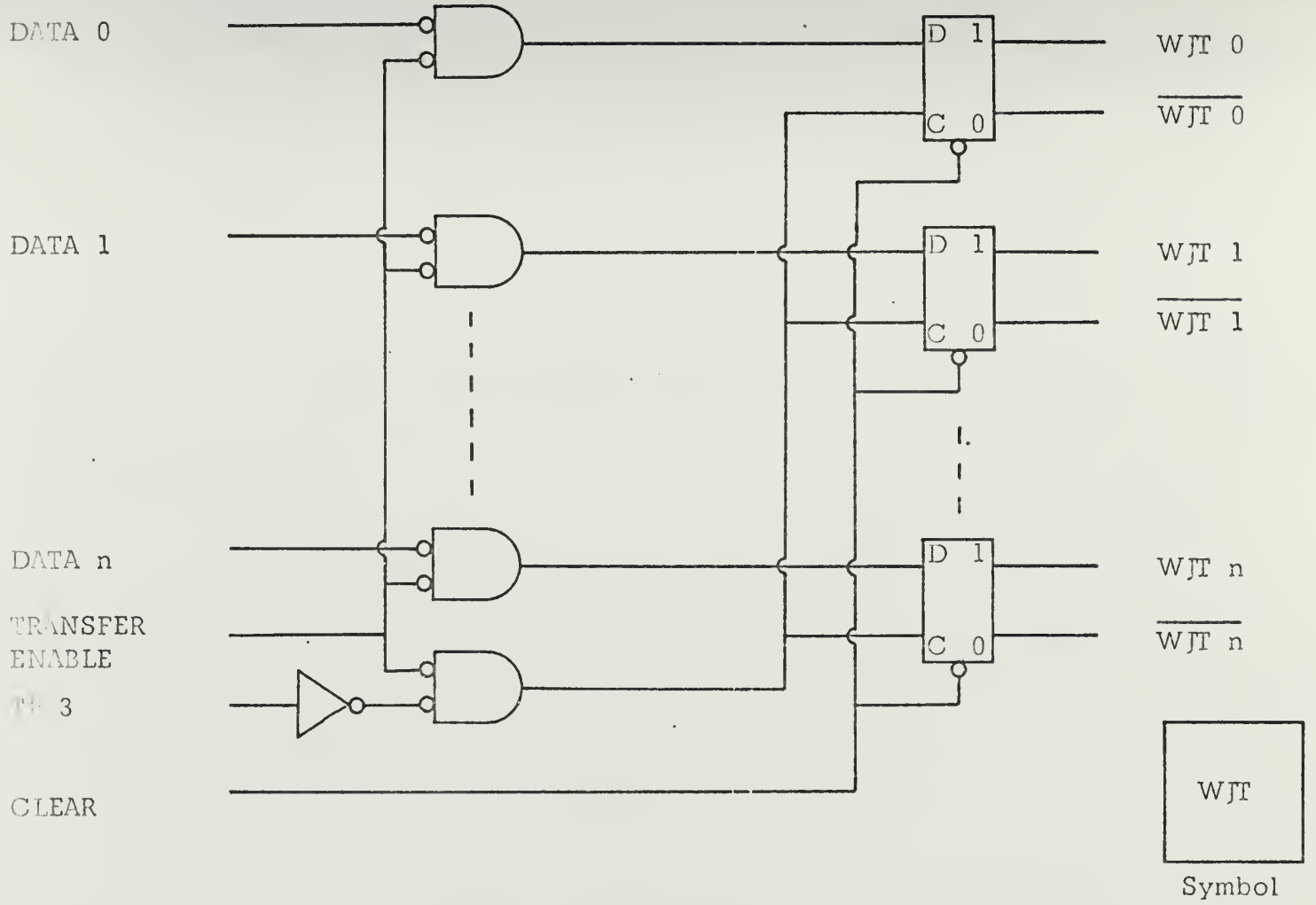


Figure 8. Word Jam Transfer

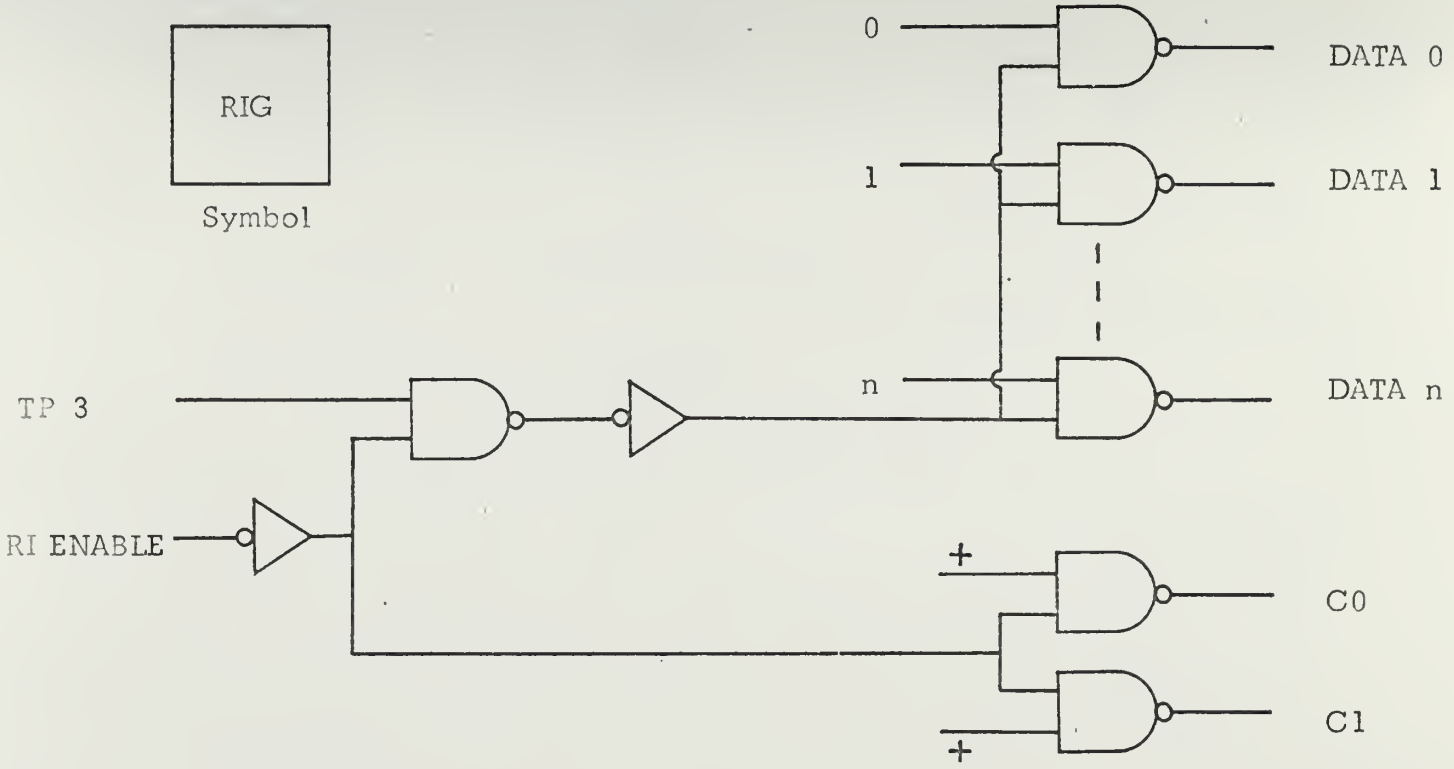


Figure 9. Read-In Gating

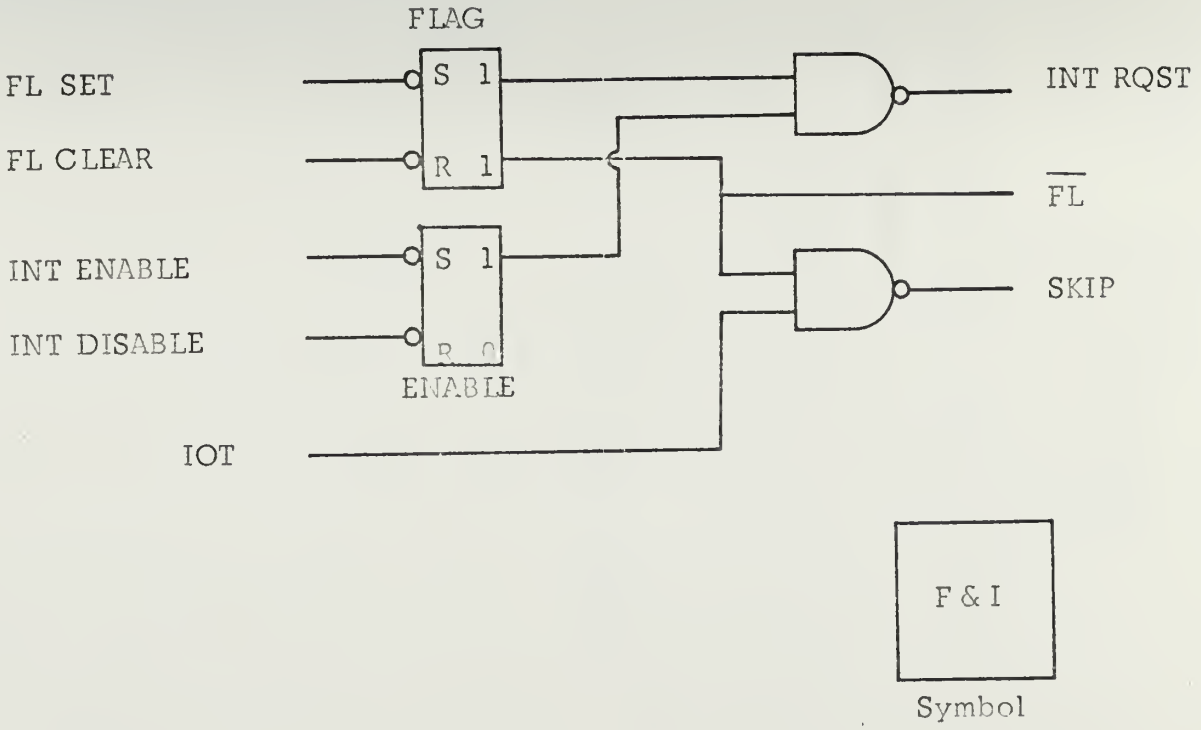


Figure 10. Flag and Interrupt

6. Inhibit Gating

The Inhibit Gating module compares two sets of inputs. OK is asserted low if all of the second input set is asserted hi and at least one of the first input set is asserted hi. Otherwise the signal will be inhibited. (Figure 11)

7. Push Down Counter

Input to the Push Down Counter is stepped through the JK flip-flops by the trailing edge of a positive-going pulse. A CLEAR is provided and information may be taken from any of the flip-flops. (Figure 12)

With these modules and special timing and control circuits, an interface may be designed without considering many of the details that might be confusing. A detail of proper signal levels between modules is created, but it is not a serious problem.

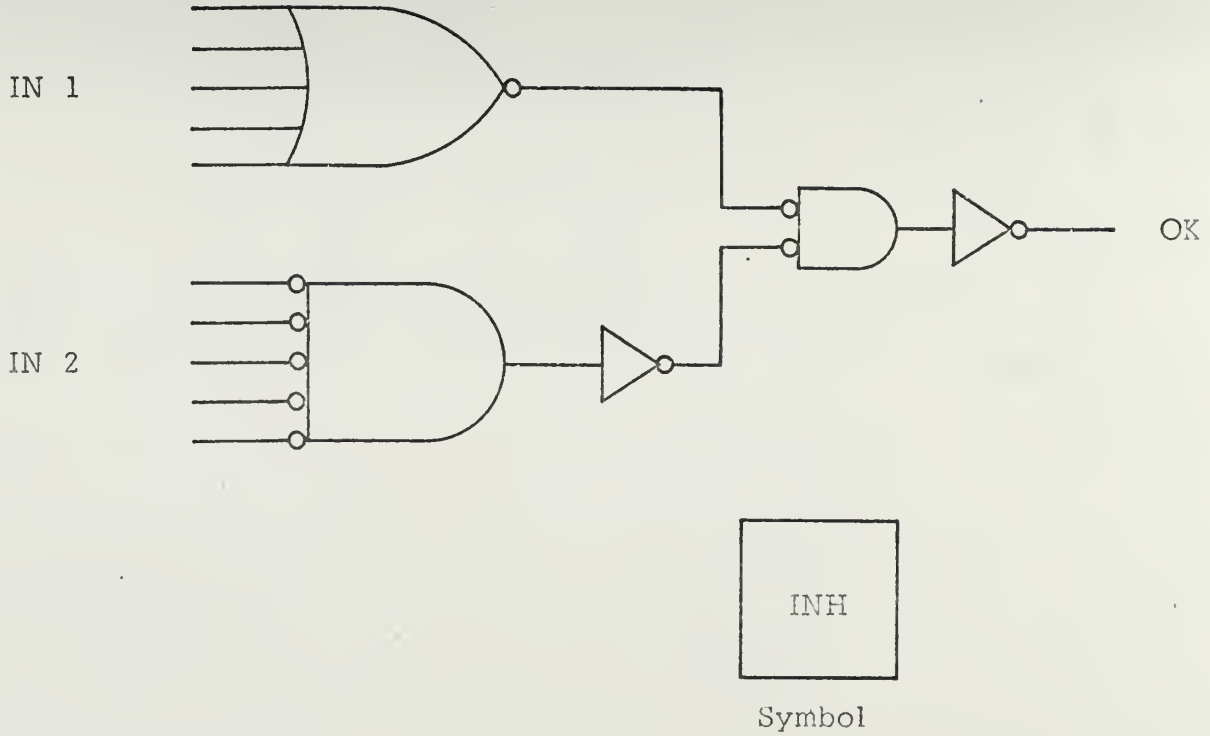


Figure 11. Inhibit Gating

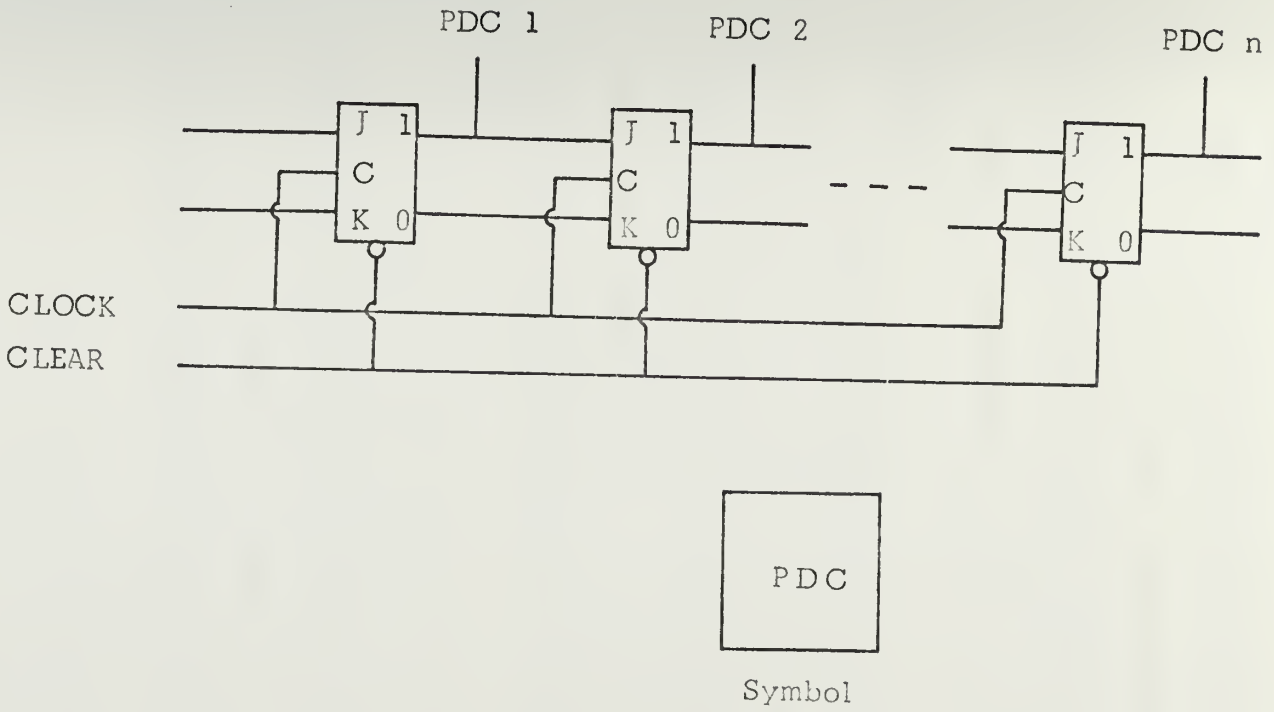


Figure 12. Push Down Counter

V. SYSTEM DESIGN

A. GENERAL

The system design integrates the five research instruments and the PDP 8/E computer. The major building blocks are the function modules set forth in the previous chapter. Additional timing and control circuits are sometimes needed to solve special problems in particular interface designs.

An overall view of the system is illustrated in Figure 13. Four of the five research instruments only send information to the computer; the human factors panel both sends and receives. Three of the instruments have analog signals that may be sampled by the A/D converter and multiplexer after appropriate modification to match voltage and impedance levels.

A summary of signals listed in Table III indicates the number and type of signal lines connected with each instrument. The human factors panel has the major number of lines to be connected to the computer, and, therefore, requires the largest part of the digital interface.

Table III

Summary of Signal Lines of the Instruments

Instrument	Number of Lines From	To	Type
polygraph	4		analog
Lifecycle	3		analog
treadmill	1		analog
pupilometer	9		analog

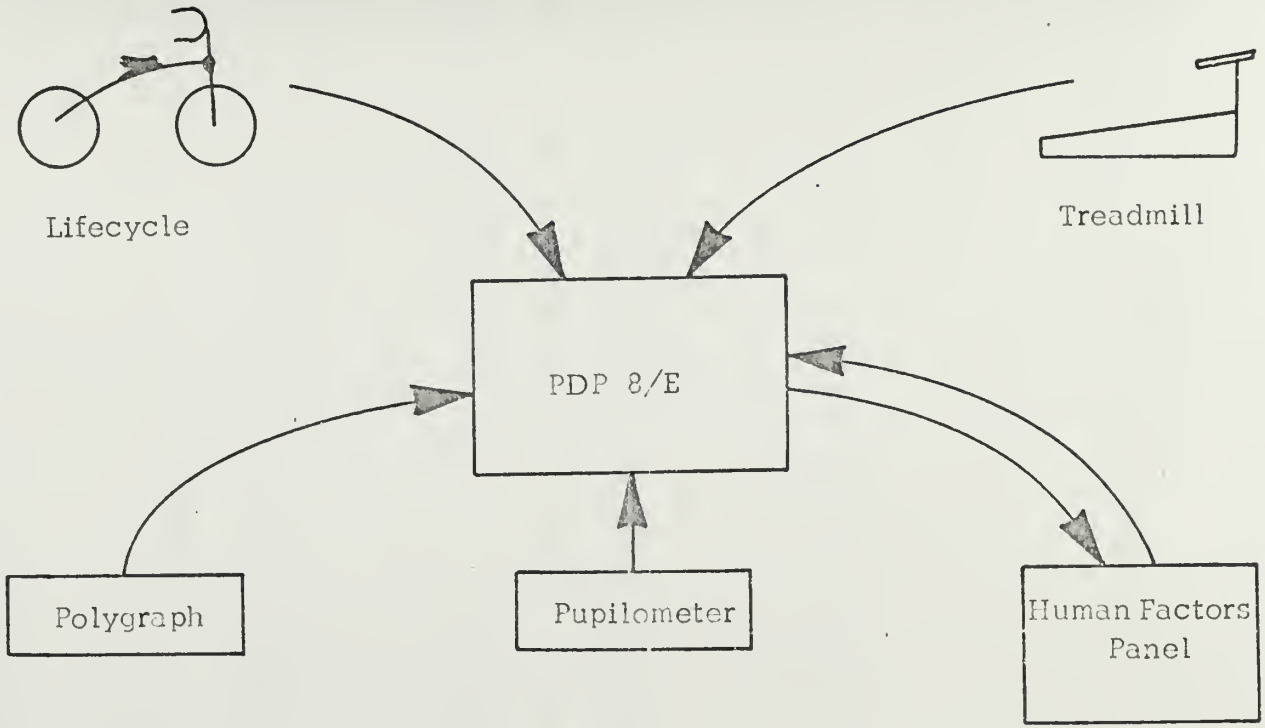


Figure 13. Human Factors System

Table III (cont)

Instrument	Number of Lines From	To	Type
human factors panel			
1. telephone dial and switch	2		digital
2. dual 12 stimulus readout and switch	1	12	digital
3. 3X4 lighted key array	12	12	digital
4. 3X4 light array		12	digital
5. nonsense syllable panel		36	digital
6. score panel (digital counter and lamp)		2	digital
7. coin dispenser		2	digital

B. PUPILOMETER

The interface for the pupilometer (Figure 14) holds the 8 bit word indicating pupil diameter, requests an interrupt, and transmits the word to the accumulator on command.

The pupilometer clocks the word into a Word Program-Timed Transfer module with a positive pulse of 1.8 μs. The pulse is inverted and sets the flag requesting an interrupt. The program goes into a service routine which chooses the device and IOT code to gate the word onto the Data Bus and asserts the proper control lines to send the word to the accumulator. IOT's are then generated to clear the interface memory and flags in preparation for another transfer.

C. HUMAN FACTORS PANEL

The seven components are considered independently to simplify the interface design.

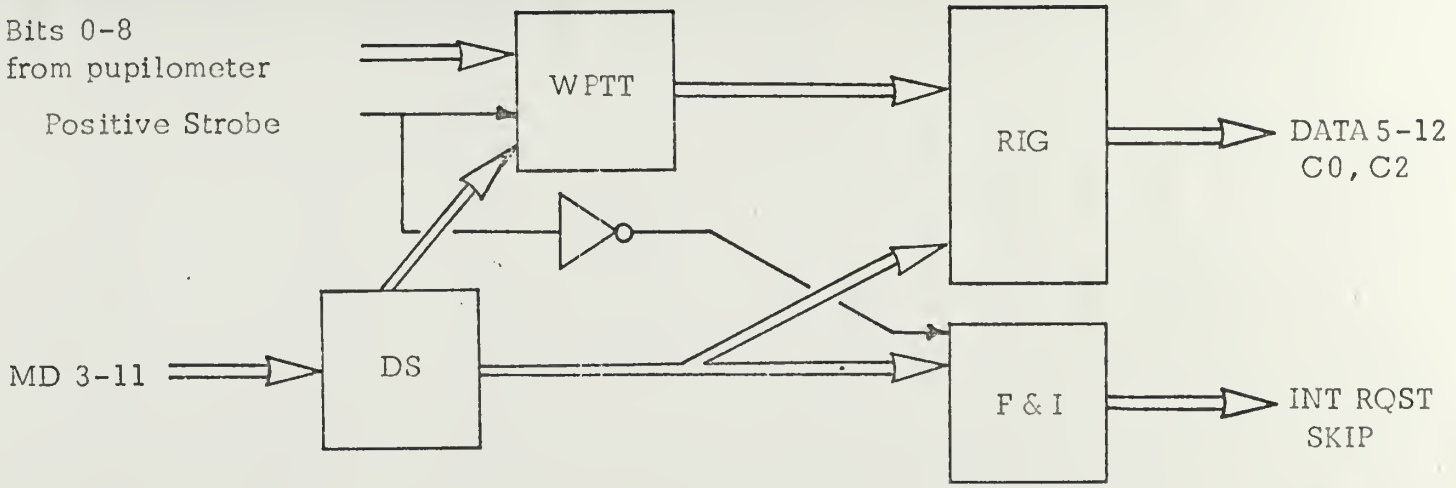


Figure 14. Pupilometer Interface

1. Telephone Dial and Switch

The at-rest switch sets an initial condition for the push-down counter. The pulses from the dial steps a 1 state through the counter. Since the input to the counter is set to 0 on the first pulse (slightly delayed), the position of the 1 in the counter indicates the number dialed. After the dial comes to rest and closes the at-rest switch, the flag is set to request an interrupt and the interface is serviced and reset. (Figure 15)

2. Dual Stimulus and Switch

Under program control data is loaded into the memory of the Word Jam Transfer module. The signals are then transferred to proper voltage levels lighting the stimulus lights. The response switches set flip-flops in the WPTT module. The Inhibit module prevents the flag from being set until the switches have been released. When the flag is set, an interrupt request is made and the bits are transferred under program control. (Figure 16)

3. 3X4 Lighted Key Array

The key array's interface is similar in concept to the stimulus and switch interface; only the size and number of modules are different. The program guides data to the interface to turn on the lights and the responses are collected and read-in using the program interrupt method. (Figure 17)

4. 3X4 Light Array

The light array interface is identical to part of that used with the lighted key array. Under program control, data is transferred to the

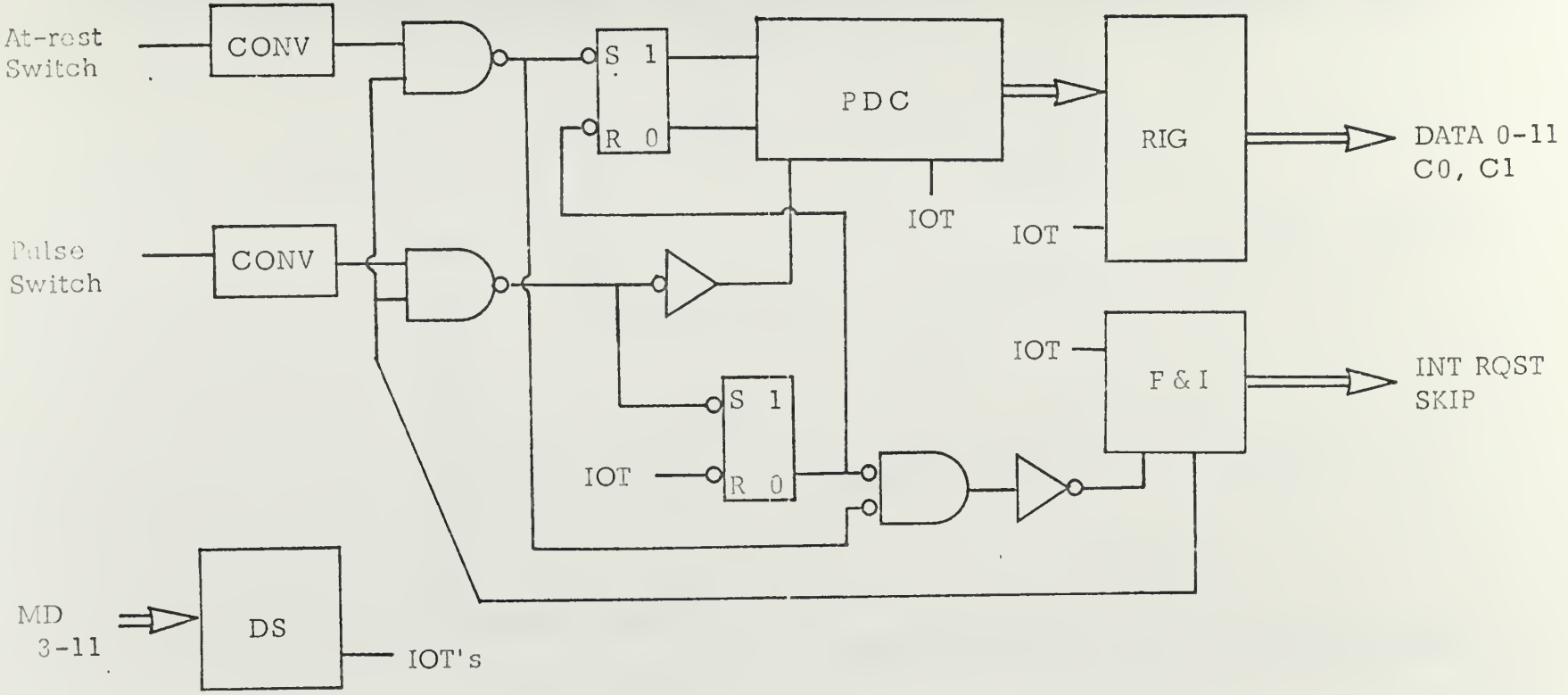


Figure 15. Telephone Dial and Switch Interface

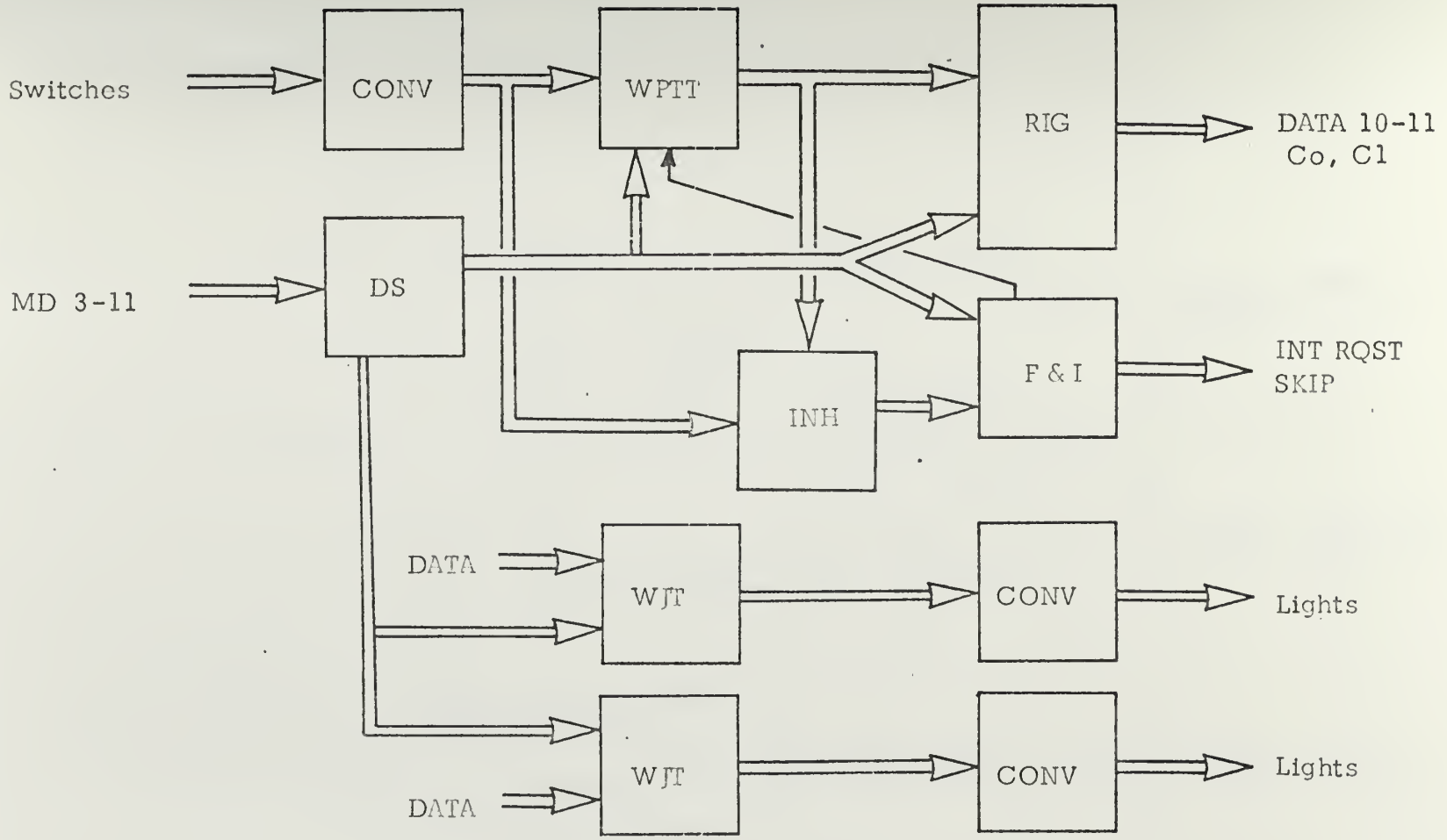


Figure 16. Dual Stimulus and Switch Interface

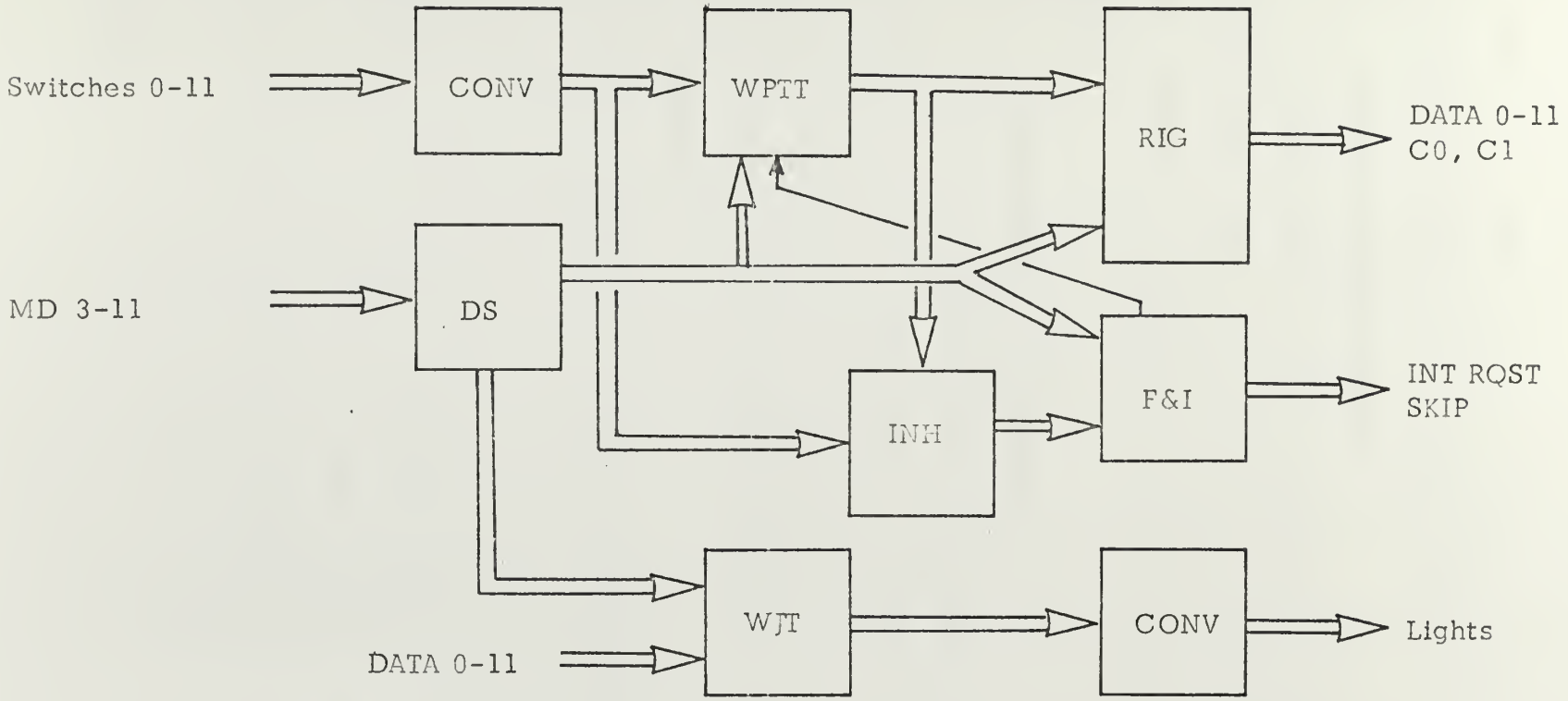


Figure 17. 3X4 Lighted Key Array Interface

peripheral to turn-on the proper lights. The length of time and how the set of lights are changed, whether turned off or replaced with a different set, are under the control of the computer. (Figure 18)

5. Nonsense Syllable Panel

The nonsense syllable panel consists of three digital read-outs with 12 states each. The interface is identical to the previous interface multiplied by 3 except for the device selector modules. (Figure 19)

6. Score Panel and Coin Dispenser

The last two panels have 2 lines each to be controlled, so they are lumped together. Again this is a simple transfer to lights or a device requiring a single pulse. Also again only the device selector, word jam transfer, and set of converter modules are used in the interface device. (Figure 20)

It can be seen that in the interface being discussed, two types of signals appear, analog and two state digital. In the case of analog signals, the signals must be converted to meet the voltage and impedance input levels of the computer. The digital signals can be manipulated with the use of the logic modules to meet computer requirements. If additional instruments and devices were added to the system, the interface could be added in units of modules particular to the device considered.

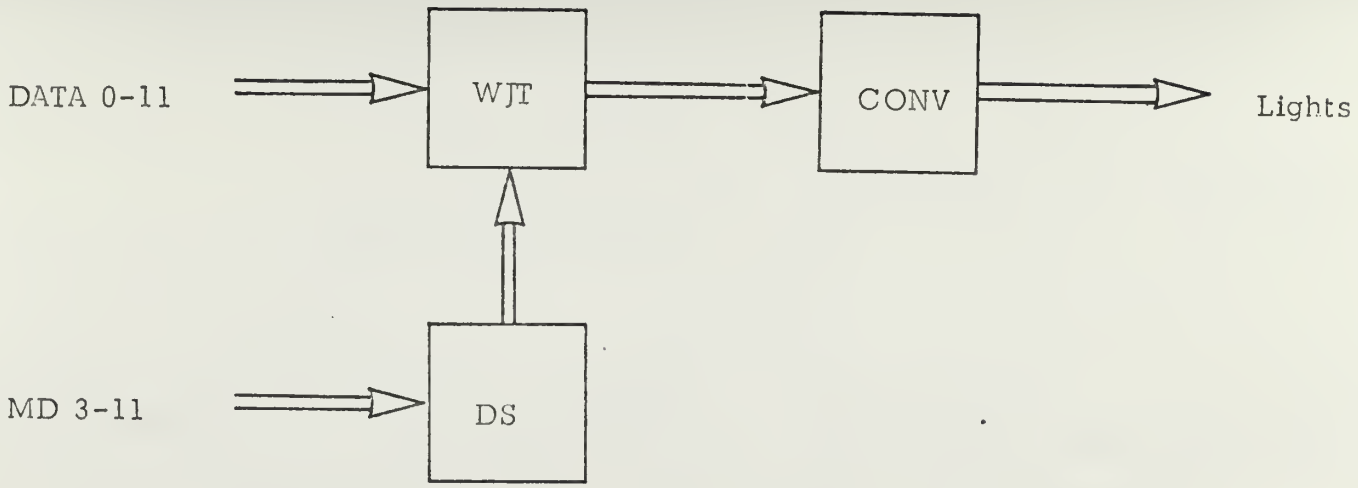


Figure 18. 3X4 Light Array Interface

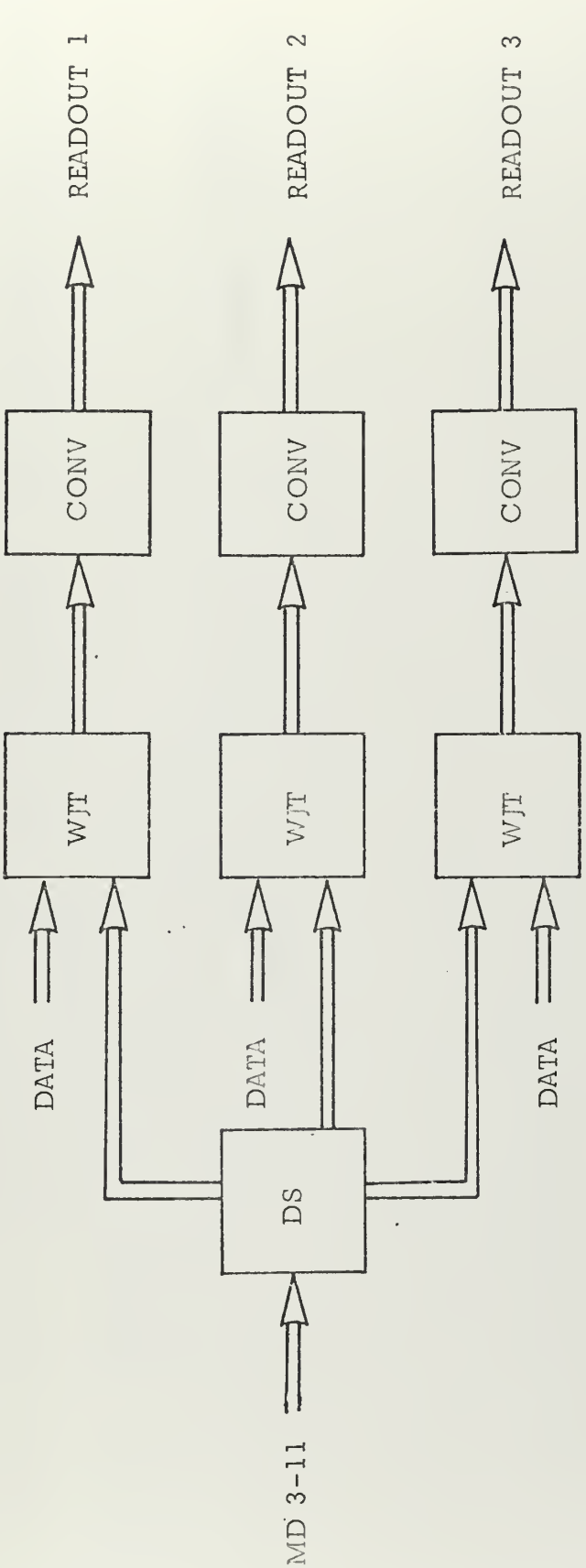


Figure 19. Nonsense Syllable Panel Interface

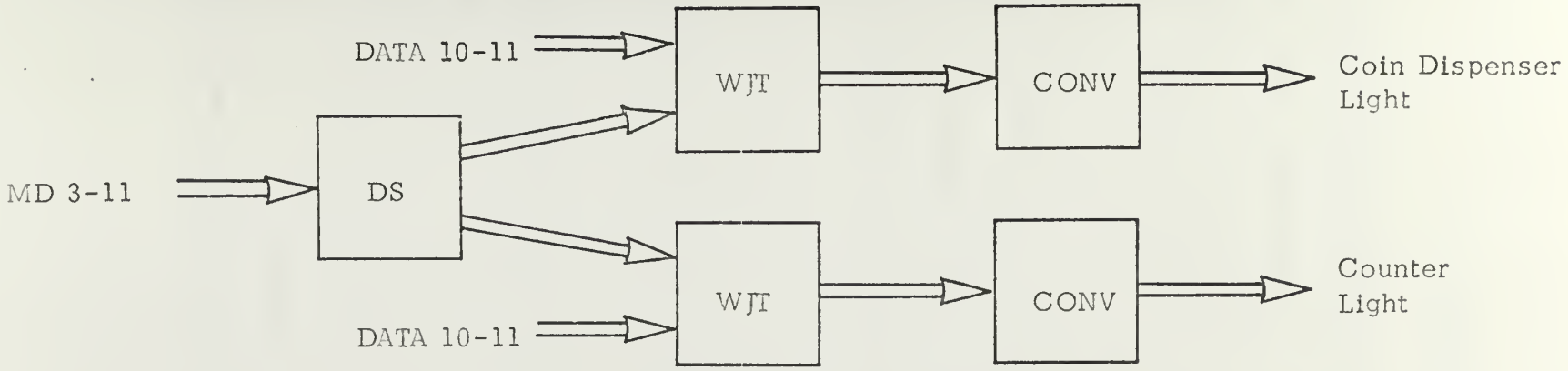


Figure 20. Score Panel and Coin Dispenser Interface

VI. CONCLUDING REMARKS

This thesis has discussed the design of a system interface to link five research instruments of a human engineering laboratory to a digital computer. It is intended that this interface be implemented in the near future. In order to do this, it will be necessary to produce schematics using logic elements alone. With these, any repetition of elements or useless elements can be detected and eliminated. (These unneeded elements can appear due to the general nature of the function modules.) Inconsistencies, such as inverted signals, can also be corrected at that time.

It may be possible to achieve some economies by grouping laboratory devices with similar characteristics together and designing an interface to service these devices as one. This was done with score panel and coin dispenser (as illustrated in Figure 20). The grouping can reduce the number of modules by not requiring more than one device selector, inhibit gating, or flag and interrupt module for the group.

A computerized system as described here with proper programming should allow an experimenter to conduct a variety of studies with accuracy and a relatively hands-off condition.

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13. ABSTRACT
The design of a system interface for a PDP 8/E computer system and the research instruments of the Human Engineering Laboratory at the Naval Postgraduate School is discussed. Emphasis is on the digital logic where a modular approach is used. Each module is a common grouping of logic elements for performing a particular function. Seven function modules are described, and their integration into a complete system is discussed. It is intended that the equipment be built and the system tested in the near future.

KEY WORDS	LINK A		LINK B		LINK C	
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